IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

2833/A1B
6/19/01
Sunder

In re application of

ROBERT H. HAVEMANN ET AL.

Serial No. 09/216,214 (TI-21570)

Filed December 18, 1998

For: ENHANCEMENTS TO POLYSILICON GATE

Art Unit 2811

Examiner T. Tran

Commissioner for Patents
Washington, D. C. 20231

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 8 to 10, 12, 14, 16, 18, 20, 22, 24, 26 and 27, all of the rejected claims. No claims have been allowed and the divisional application Serial No. 09/262,512 which is directed to the method has been allowed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after a second or subsequent rejection.

SUMMARY OF INVENTION

The invention relates to a transistor structure, the structure including a gate dielectric (10, 10') over a semiconductor region (not numbered and disposed under the gate dielectric). A patterned gate (20) is disposed over the gate dielectric and has sidewalls (metal 50 and silicide 60), a top surface remote from the gate dielectric and a bottom surface disposed on the gate dielectric. The gate dielectric includes, as a part thereof, a lateral growth at the corners of the gate, but not under central regions of the gate, the thickness of the gate dielectric continually increasing at the interface of the bottom surface and the sidewalls of the gate in a direction from the bottom surface toward and along the sidewalls (the portion of gate dielectric 10' not existing in gate dielectric 10 as shown in Fig. 2B). A unitary electrically conductive metallic material (60) entirely covers the sidewalls and top surface of the gate. Source and drain regions (80) in the semiconductor region define a channel (region in unnumbered substrate between regions 80/70) under the patterned gate.

According to a second feature of the invention, a transistor structure is provided having a region of semiconductor material (not numbered) having a gate dielectric (10, 10') thereover. A polysilicon gate (20) is disposed over the gate dielectric, the gate having a top, a bottom and sidewalls. A silicide layer (60) is disposed on the top and sidewalls of the polysilicon gate and source/drain regions (80) are disposed in the region of semiconductor material spaced apart from each other, adjacent to and aligned with the silicide layer disposed on the sidewalls. The transistor structure can include a lightly doped source/drain extension 70 of each of the source/drain regions extending under the polysilicon gate. The transistor structure can still

further include a dielectric (portion of 10' not found in dielectric 10) extending from the gate dielectric of increased thickness relative to the gate dielectric and disposed under the silicide layer. The silicide layer extends to the gate dielectric. of increased thickness

ISSUES

The issues on appeal are as follows:

1. Whether claims 8 and 9 would be objected to as being informal.

2. Whether claim 10 claims subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention under 35 U.S.C. 112, first paragraph.

3. Whether claims 8 and 9 are definite under 35 U.S.C. 112, second paragraph.

4. Whether claims 8 to 10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 are patentable over Arai (U.S. 5,841,174) in view of Watabe et al. (U.S. 4,727,038) or Tada (JP 4-42938).

GROUPING OF CLAIMS

The claims do not stand or fall together for reasons set forth hereinbelow under ARGUMENT.

ARGUMENT

ISSUE 1

Claims 8 and 9 were objected to as being informal because the Examiner is of the opinion that the term "said gate" should be --said patterned gate--. The objection is without merit.

The objection is in fact tantamount to a rejection on the ground of indefiniteness under 37 C.F.R. 1.112, second paragraph. The legal standard for definiteness is whether a claim reasonably apprised those of skill in the art of its scope. See, for example, Amgen Inc. v. Chugai

Pharmaceutical Co. Ltd. 18 USPQ2d 1016, 1030 (Fed. Cir.)" as stated in In re Warmerdam, 31 USPQ2d 1754 at 1759. A review of claims 8 and 9 immediately reveals that only one gate is mentioned, this gate being a "patterned gate". However, since only one gate is mentioned, reference back using the term "gate" alone is clear and definite and indicates even to one unskilled in the art that the only gate mentioned must be the one being referenced. It follows that the objection is without merit.

ISSUE 2

Claim 10 was rejected under 35 U.S.C. 112, first paragraph, as claiming subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention under 35 U.S.C. 112, first paragraph. In this regard, the Examiner states that "[t]he recitation of source/drain regions each disposed adjacent to and aligned with the silicide layer disposed on the sidewalls in claim 10 can be interpreted as setting forth structure not supported by the specification. The specification and Fig. 2D support a structure with source/drain regions (70,80) formed by implantation and diffusion to disperse the dopants. As a result, the source/drain regions are not aligned with the silicide layer 60." The rejection is without merit as will be demonstrated.

Reference is initially invited to the first full paragraph on page 8 of the specification wherein, prior to silicide formation 60 as shown in Fig. 2D and after conformal deposition of the side wall metal 50 as shown in Fig. 2C, it is stated at line 7ff that "the source/drain areas receive their final doping, which is implanted (step 145) through the layer of metal to form regions 80. It is noted that the conformal metal on the sidewalls of the gate acts to mask that portion of the substrate from receiving this implant" (underline not in original). As is well known in the art as well as

readily apparent from common sense, since the portion of the substrate under the gate and sidewalls is masked, the source/drain regions 80 are formed to the side of the sidewalls and are therefore in alignment with the silicide layer (which is merely the metal layer 50 converted to the silicide 60). It follows that claim 10 and the subject matter therein are fully set forth in the specification as filed as would be apparent to the ordinary artisan and is certainly apparent to one skilled in the art to which this invention pertains.

ISSUE 3

Claims 8 and 9 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. In this regard, the Examiner objects to the use of "said gate" in lines 5, 6, 7 and 10 of each claim and to the use of "the thickness" in line 6 of each claim. As stated above, the legal standard for definiteness is whether a claim reasonably apprised those of skill in the art of its scope. See Amgen Inc. v. Chugai Pharmaceutical Co. Ltd. 18 USPQ2d 1016, 1030 (Fed. Cir.)" as stated in In re Warmerdam, 31 USPQ2d 1754 at 1759.

The argument as to the definiteness of the term "said gate" is set forth above with reference to Issue 1 and that argument is incorporated herein by reference.

With reference to the term "the thickness" in line 6 of claims 8 and 9, the dielectric, being a thin sheet, has only one effective principal dimension, this dimension being the distance between the substrate (not numbered and shown in part in Figs. 2C and 2D as having regions 70 and 80 therein)on which the dielectric layer 10 is formed and the gate region 20. The other two dimensions are generally based upon the area covered by the array of active components and is therefore not a principal dimension since it has no effect on the circuitry itself. It follows that the language is clear and definite in accordance with the requirements of the above cited cases from the Federal Circuit.

ISSUE 4

Claims 8 to 10, 12, 14, 16, 18, 20, 22, 24, 26 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Arai (U.S. 5,841,174) in view of Watabe et al.(4,727,038) or Tada (Japan 4-42938). The rejection is without merit.

It is initially noted that the Examiner has challenged the manner in which appellants have argued the rejection in the last paragraph on page 6 of the last Office action (dated March 6, 2001) and it is believed that this challenge requires a rebuttal. It is respectfully submitted that by arguing in the exact terms of the claims, the argument could not be more distinct and specifically point to the errors in the Office action. In arguing in the terms of the claims appellants have specifically stated that which is not shown by the cited art either alone or in the combination as claimed. The burden then is shifted to the Examiner. As is apparent from the taking of this appeal, appellants believe that this burden has not been met by the Examiner.

Claims 8 and 9 require, among other features, a lateral growth on the gate dielectric at the corners of the gate, but not under central regions of the gate, the thickness of the gate dielectric continually increasing at the interface of the bottom surface and the sidewalls of the gate in a direction from the bottom surface toward and along the sidewalls. This provides increased gate conductivity, additional control over gate corner profiles, additional control over gate electric fields, additional control over silicided gate structures and additional control over the line-to-space ratio of the gate pattern, while using conventional processing techniques. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references taken alone or in the combination as claimed.

The Examiner states that the term "lateral growth" is a product by process limitation and is given no patentable weight. This allegation is incorrect. While appellants agree that a product

by process limitation need not be given patentable weight, the term "lateral growth" is not such a limitation. A lateral growth on the gate dielectric is a physical and not a process limitation and refers to the regions of the dielectric layer 10 (shown as 10' after the lateral growth) which have grown after oxidation. This is fully discussed at page 7 of the specification wherein it is stated at lines 23ff "[o]nce the gate is covered with nitride, an oxidation is performed (step 120), which makes the gate oxide 10' wider under the gate corners than it is near the center of the gate. This is often called a 'smiling oxidation', due to the creation of upturned corners in the oxide".

The Examiner challenges the arguments presented in stating that the alignment of the source/drain regions is not found in the disclosure as originally filed and that Fig. 2D clearly shows source/drain regions 80 not aligned with the silicide layer. These allegations are contrary to fact. The alignment is found in the disclosure as originally filed as demonstrated above in connection with the argument as to Issue 2. As to the drawings, it is elementary in the case law that the drawings are not to scale and can be given no weight in this regard. Furthermore, as demonstrated above in connection with the argument as to Issue 2, the source/drain regions 80 are aligned and must be aligned with the silicide as well as the metal that forms the silicide. Note at page 8, lines 9 to 11 it is clearly stated "[i]t is noted that the conformal metal on the sidewalls of the gate acts to mask that portion of the substrate from receiving this implant" when referring to the source/drain implant 80. This is a clear statement that the dopant (i.e., the source/drain region precursor) does not travel under the gate region or the sidewall metal or silicide and is therefore aligned with the sidewall metal or silicide. No other logical conclusion is possible.

Claim 10 requires, among other features, a silicide layer disposed on the top and sidewalls of the polysilicon gate and source/drain regions in the region of semiconductor

material spaced apart from each other and each disposed adjacent to and aligned with the silicide layer disposed on the sidewalls. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references taken alone or in the combination as claimed.

Claims 12, 14, 16, 18, 20, 22, 24, 26 and 27 depend from claim 10 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 10.

Claim 12 further limits claim 10 by requiring that the silicide layer be titanium silicide. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references in the combination as claimed.

Claims 14 and 16 further limit claims 10 and 12 by requiring a lightly doped source/drain extension of each of the source/drain regions extending under the polysilicon gate. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references in the combination as claimed.

Claims 18, 20, 22 and 24 further limit claims 10, 12, 14 and 16 by requiring a dielectric extending from the gate dielectric of increased thickness relative to the gate dielectric and disposed under the silicide layer. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references either alone or in the combination as claimed.

Claim 26 further limits claim 10 by requiring that the silicide layer extend to the gate dielectric. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references either alone or in the combination as claimed.

Claim 27 further limits claim 18 by requiring that the silicide layer extend to said dielectric of increased thickness. No such arrangement is taught or suggested by Arai, Watabe et al., Tada or any proper combination of these references either alone or in the combination as claimed.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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APPENDIX

The claims on appeal read as follows:

8. A transistor structure, comprising:

(a) a gate dielectric over a semiconductor region;

(b) a patterned gate over said gate dielectric having sidewalls, a top surface remote from said gate dielectric and a bottom surface disposed on said gate dielectric;

(c) a lateral growth on said gate dielectric at the corners of said gate, but not under central regions of said gate, the thickness of said gate dielectric continually increasing at the interface of said bottom surface and said sidewalls of said gate in a direction from said bottom surface toward and along said sidewalls;

(d) a unitary electrically conductive metallic material entirely covering said sidewalls and top surface of said gate; and

(e) source and drain regions in said semiconductor region defining a channel under said patterned gate.

9. A transistor gate structure, comprising:

(a) a gate dielectric over a semiconductor region;

(b) a patterned gate over said gate dielectric having sidewalls, a top surface and a bottom surface disposed on said gate dielectric;

(c) a lateral growth on said gate dielectric at the corners of said gate, but not under central regions of said gate, the thickness of said gate dielectric continually increasing at the interface of said bottom surface and said sidewalls of said gate in a direction from said bottom surface toward and along said sidewalls; and

(d) a unitary electrically conductive metallic material entirely covering said sidewalls and top surface of said gate.

10. A transistor structure which comprises:

a region of semiconductor material having a gate dielectric thereover;

a polysilicon gate disposed over said gate dielectric having a top, a bottom and sidewalls;

a silicide layer disposed on said top and sidewalls of said polysilicon gate; and

source/drain regions in said region of semiconductor material spaced apart from each other, said source/drain regions each disposed adjacent to and aligned with said silicide layer disposed on said sidewalls.

12. The transistor structure of claim 10 wherein said silicide layer is titanium silicide.

14. The transistor structure of claim 10 further including a lightly doped source/drain extension of each of said source/drain regions extending under said polysilicon gate.

16. The transistor structure of claim 12 further including a lightly doped source/drain extension of each of said source/drain regions extending under said polysilicon gate.

18. The transistor structure of claim 10 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

20. The transistor structure of claim 12 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

22. The transistor structure of claim 14 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

24. The transistor structure of claim 16 further including a dielectric extending from said gate dielectric of increased thickness relative to said gate dielectric and disposed under said silicide layer.

26. The transistor structure of claim 10 wherein said silicide layer extends to said gate dielectric.

27. The transistor structure of claim 18 wherein said silicide layer extends to said dielectric of increased thickness.